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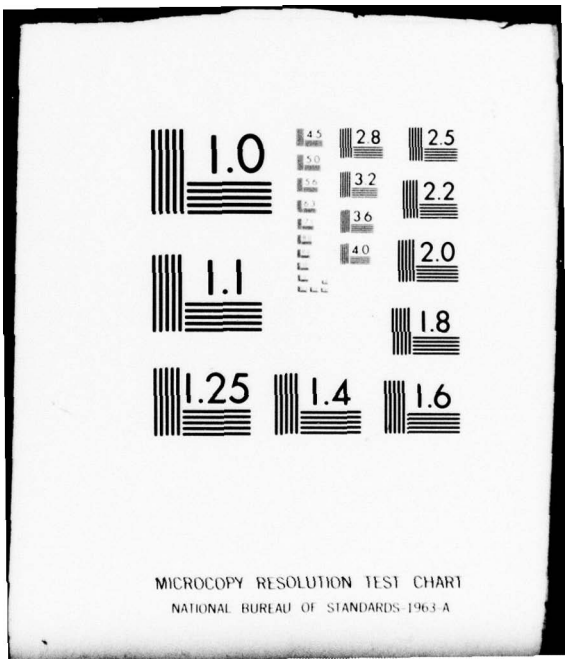
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J. G. Oakes, V. L. Wrick and R. A. Wickstrom

Final Report
For Period Ending August 1978

Contract No. N00014-76-C-0735
General Order No. WGD-10618-CE

Contract Authority NR 251-022

Prepared for
Office of Naval Research
Arlington, VA

Westinghouse R&D Center
1310 Beulah Road
Pittsburgh, Pennsylvania 15235

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necessary, resulting in some depletion mode action by the JFET. The high forward biased gate voltage of these devices, 2-3 volts, was the result of a rectifying contact on the p-type $Al_xGa_{1-x}As$ and not due to the anticipated larger work function difference. The devices showed a cut-off frequency, f_{max}, of 1.5 GHz.

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SUMMARY

An enhancement mode junction field effect transistor (JFET) using an $Al_xGa_{1-x}As$ gate and a GaAs channel was designed and fabricated in an attempt to establish a GaAs logic technology base permitting "direct" coupling without the necessity for level shifting, while at the same time, permitting a wider dynamic range (noise margin) due to the larger anticipated built-in voltage of the heterojunction gate. The heterojunction layers were grown by liquid phase epitaxy (LPE). Although the control of doping level and morphology was good, the GaAs layers were thicker than necessary, resulting in some depletion mode action by the JFET. The high forward biased gate voltage of these devices, 2-3 volts, was the result of a rectifying contact on the p-type $Al_xGa_{1-x}As$ and not due to the anticipated larger work function difference. The devices showed a cut-off frequency, f_{max}, of 1.5 GHz.

1. INTRODUCTION

This final report describes the work on Contract N00014-76-C-0735 which began August 1976 and ended July 1977. This was a one year effort to investigate the feasibility of fabricating junction field effect transistors (JFETs) utilizing an n-type GaAs channel and a p-type AlGaAs junction gate. When constructed such that the built-in potential of the gate junction fully depletes the GaAs channel at zero applied gate voltage, these devices could be used as high speed logic elements with no need for the level shifting circuits employed in depletion mode logic. The use of a heterojunction gate was believed to offer advantages in higher available input voltage swing and lower zero bias input capacitance.

Based on published heterojunction growth experience, a liquid-phase epitaxy (LPE) system was used to grow the double layer JFET structure. This consisted of a p-type AlGaAs layer on an n-type GaAs layer. The p-type AlGaAs was doped with Ge which provided a high acceptor concentration with little diffusion into the GaAs below. The GaAs layers were Sn doped with a thickness of 0.3 microns. Both layers were reproducibly grown on semi-insulating GaAs substrates with a good surface morphology for later photolithography steps in the JFET fabrication process.

The heterojunction gate JFET used ohmic contacts to both p-type GaAlAs and n-type GaAs as well as selective etching of the AlGaAs without removing any GaAs. The resulting devices showed enhancement operation up to ~1 volt forward gate voltage and gains of 3 dB at 1 GHz for 3-4μ gate length.

The higher forward voltage capability of the heterojunction gate FET was found consistently to be minimally larger than the forward voltage of a simple GaAs junction gate. This precluded any further development of this novel transistor for enhancement mode logic circuits. The technology which has been developed for heterojunction growth and selective etching may be useful for other devices. The heterojunction looks promising for electron confinement in the GaAs channel by using a GaAlAs buffer layer between the active channel and the substrate.

2. DEVICE DESIGN

The choice of AlGaAs/GaAs as the heterojunction materials for the JFET was based on the mobility of electrons in GaAs, the large bandgap of AlGaAs and the relative lattice match between the two materials. The high electron mobility of GaAs has long been exploited for microwave Schottky barrier gate FETs. At 10^{17} cm^{-3} doping density, the mobility of GaAs is as high as 5200 cm^2/volt-sec in liquid phase epitaxial material. This is about a factor of 5 improvement over silicon at that doping density, and results in low carrier transit time, low series resistances, and high transconductance. In addition, semi-insulating substrates for low parasitic mounting of the finished device are readily available.

The desired gate material requirements were a higher band gap than GaAs and a reasonable lattice match. A graph of the lattice constants and bandgaps of several ternary and binary III-V compounds is shown in Figure 2.1. The only compound with close lattice matching and higher bandgap is AlAs or ternary compounds of AlGaAs. The bandgap of GaAs is 1.43 eV while AlAs is nearly 2.1 eV. Growth of AlAs is not suitable, however, since the material is hydroscopic. An AlGaAs ternary alloy with the composition $Al_{.4}Ga_{.6}As$ was chosen to provide a bandgap of ~1.9 eV and a lattice mismatch of only 0.063%.

A cross section of the heterojunction gate FET structure is shown in Figure 2.2. The source and drain regions are ohmic contacts

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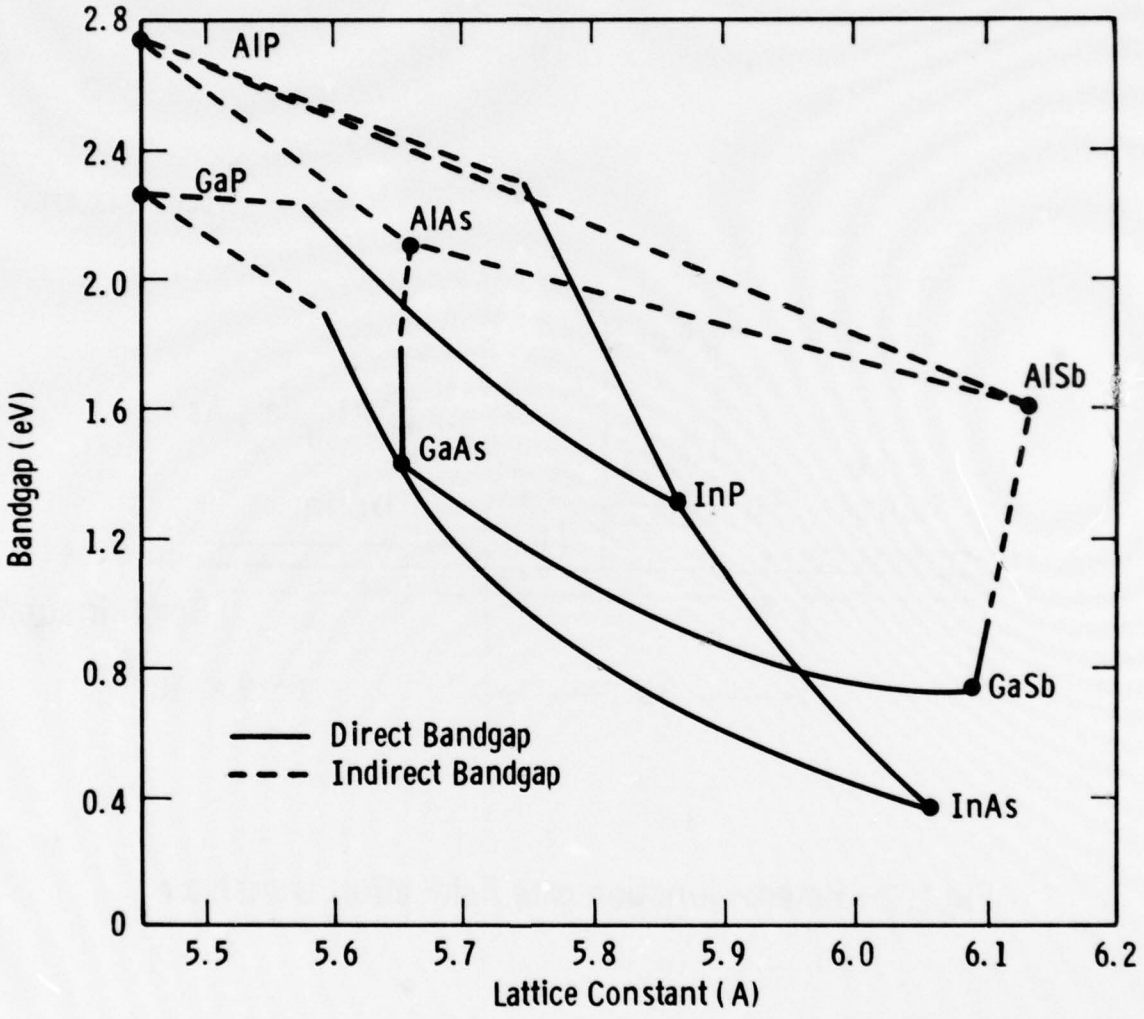

Fig. 2.1—Variation of the bandgap as a function of lattice constant for a number of ternary III-V compounds

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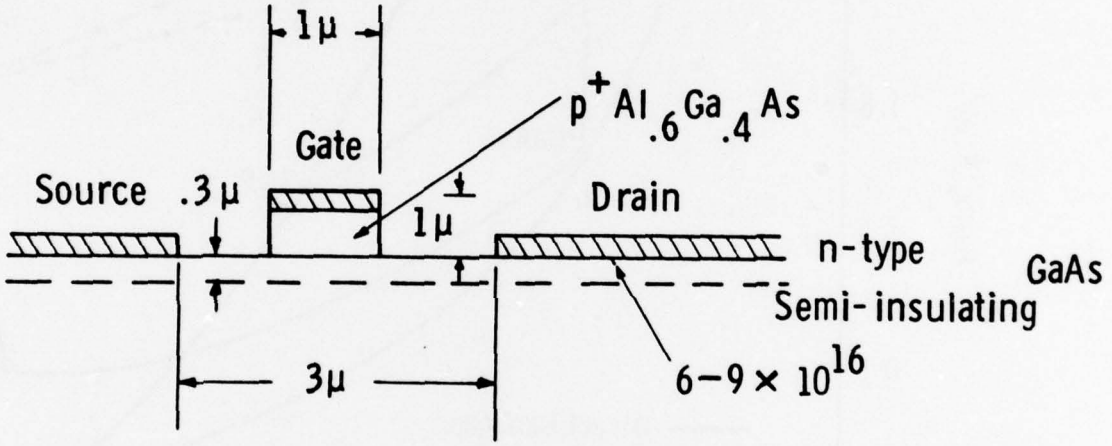

Fig. 2. 2— Hetero-junction gate field-effect transistor

to the n-type GaAs layer which covers the semi-insulating GaAs substrate. The gate electrode consists of an ohmic contact to the p-type AlGaAs which has been defined by etching to a narrow line between the source and drain. In operation, modulation of the gate to source voltage will modulate the depletion region beneath the gate and provide an amplified signal in the drain current flow. To work optimally, the p-type doping of the AlGaAs must be substantially higher than the GaAs channel doping or part of the modulating voltage will be wasted by varying the depletion in the p-type AlGaAs. In addition, the channel thickness must be thin so that the built-in potential of the heterojunction can deplete it with no applied gate voltage. This results in the "enhancement" mode operation of the FET. The required channel thickness for a channel doping of 8×10^{16} is shown for a range of built-in voltages in Figure 2.3. For a built-in voltage of 1.4V, corresponding to a GaAs homojunction, the channel thickness is only 1500Å.

The mask layout for these devices used 300 μm, 150 μm and 120 μm periphery devices to allow wire bonding of individual FET's into the basic NAND, NOR and inverter configurations. A photograph of a finished device group is shown in Figure 2.4. A total of eight JFET's are included in each group. The smaller periphery devices are used as the active loads for the 300 μm devices. The details of the logic circuit connections are shown in Figure 2.5.

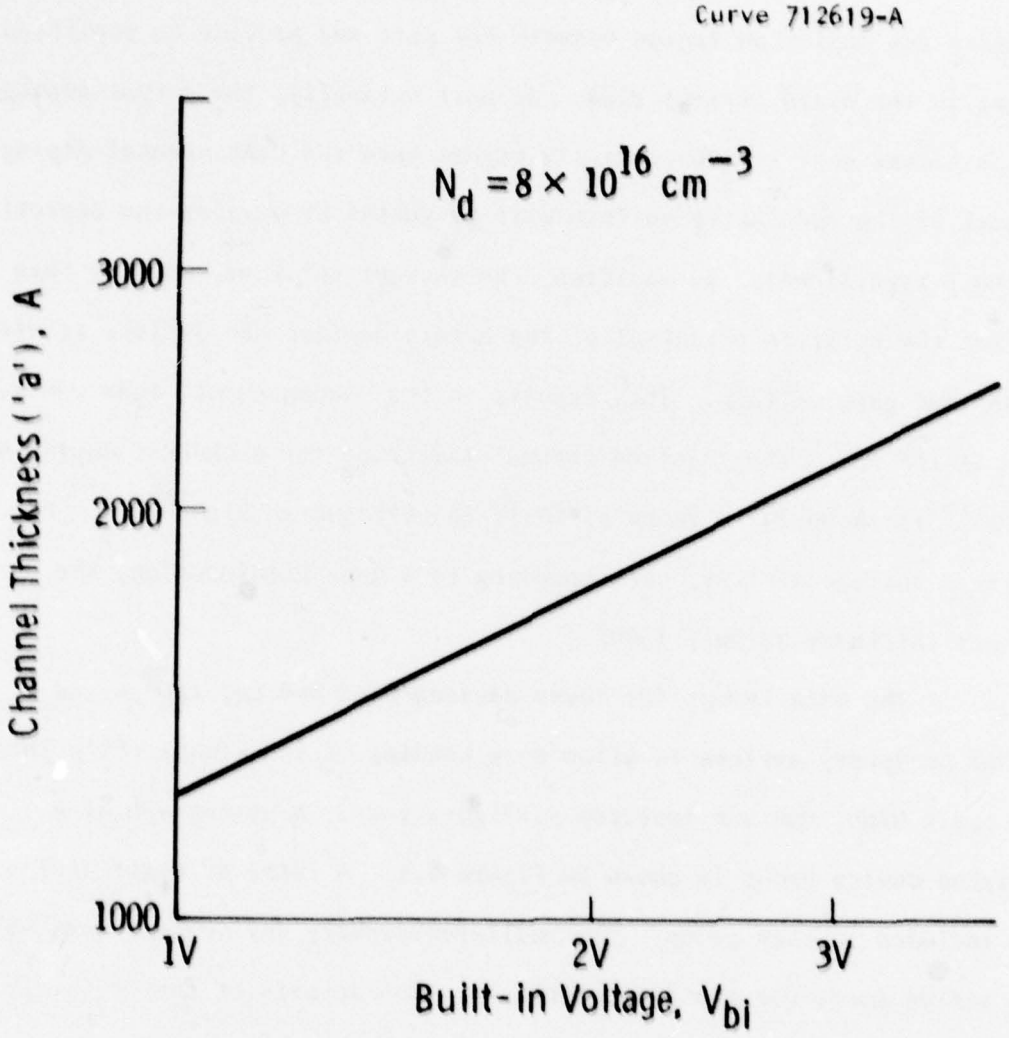

Fig. 2.3—Channel thickness variation with built-in voltage for GaAs

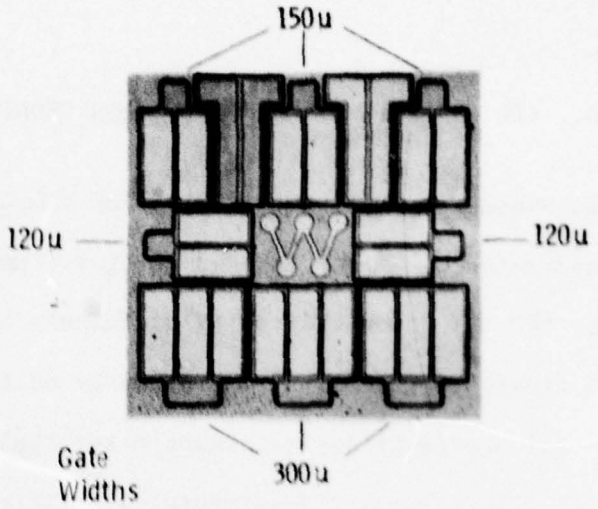

Fig. 2.4—Layout of heterojunction FETs with 300, 150 and 120 u m periphery

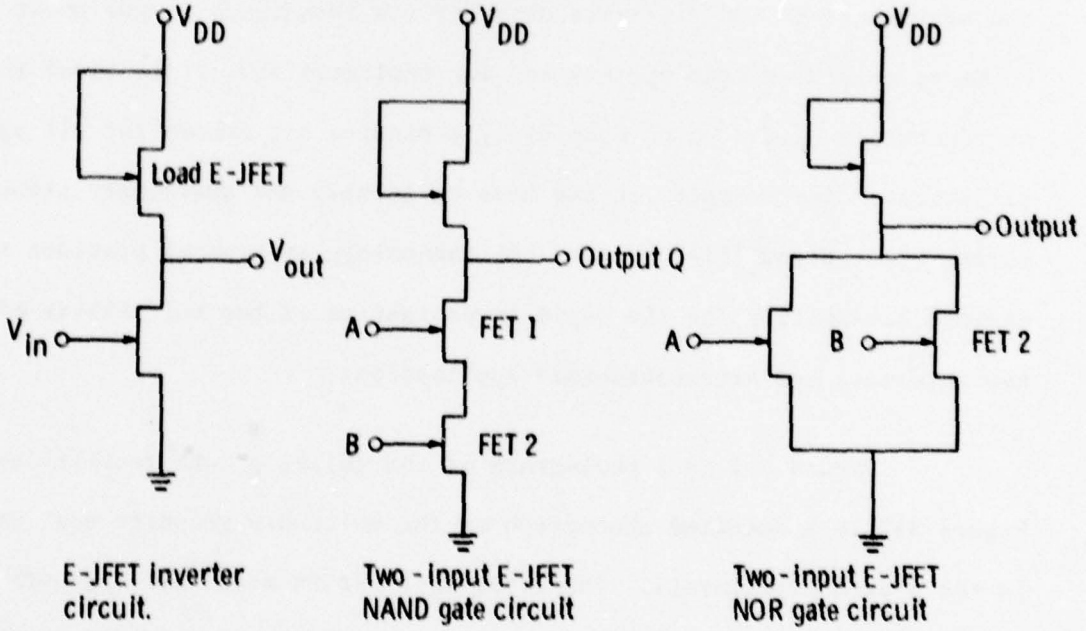

Fig. 2.5—Circuit realization of inverter, NAND and NOR functions with enhancement JFETs

3. LPE GaAs/AlGaAs HETEROJUNCTION GROWTH

Liquid Phase Epitaxial growth (LPE) of semiconductors was originally demonstrated by Nelson in 1963 using a tipping apparatus. Since that time, LPE has demonstrated its usefulness in compound semiconductor III-V growth by fulfilling a wide range of tasks including optoelectronic device production, microwave mixer applications, Gunn, IMPATT and MESFET structures and fundamental materials studies. While a significant controversy still exists regarding the relative strengths and weaknesses of LPE vis-a-vis other growth techniques (vapor phase epitaxy, molecular beam epitaxy and ion implantation), it is clear that no technology exists which completely dominates all others for all applications. Accordingly, in the area of ternary and quaternary structures, i.e., mixed III-V growth, LPE technology at present provides the maximum flexibility for the rapid investigation of the suitability of new materials and heterostructure applications.

Figure 3.1 is a photograph of the (W) LPE growth facility and Figure 3.2 is a detailed photograph of the multi-bin graphite boat used in the growth experiments. The major interest in mixed III-V growth has centered around "engineered" materials, i.e., the design of alloys with particular energy gaps advantageous for various optoelectronic applications. In addition, the properties of heterostructures are appealing for both microwave and optical devices.

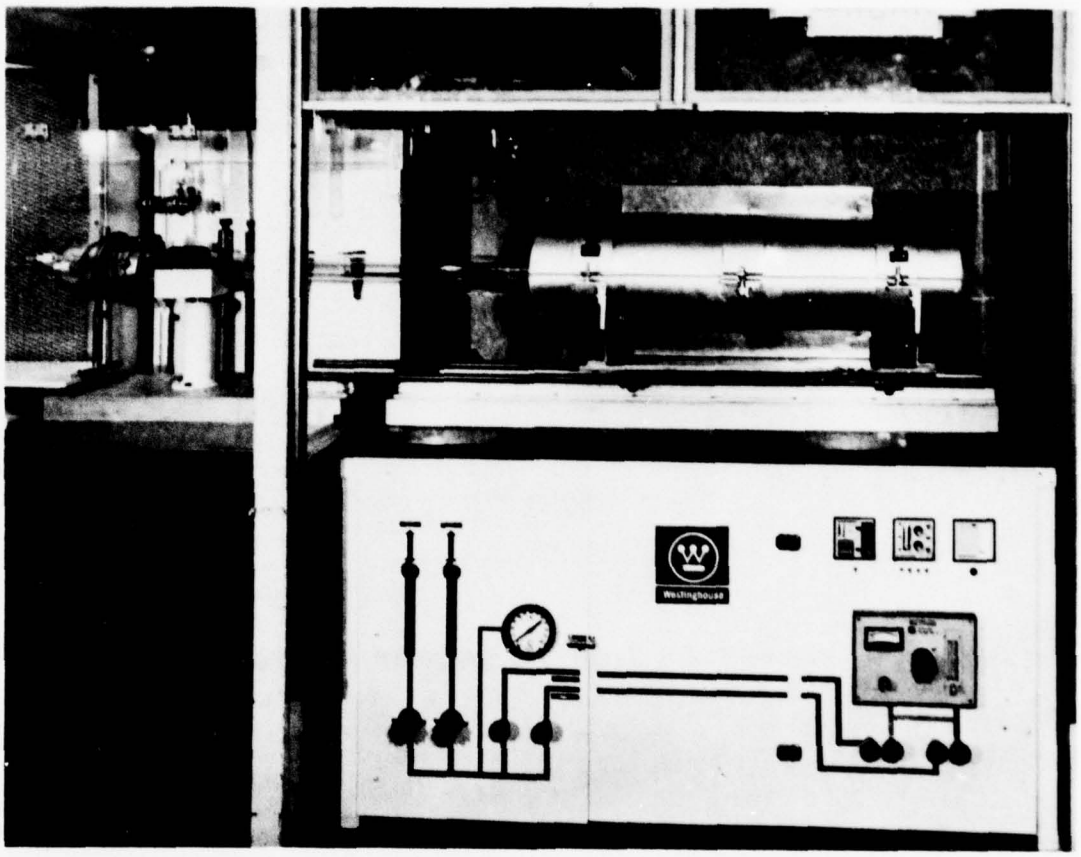

Figure 3.1 Liquid phase epitaxial growth system

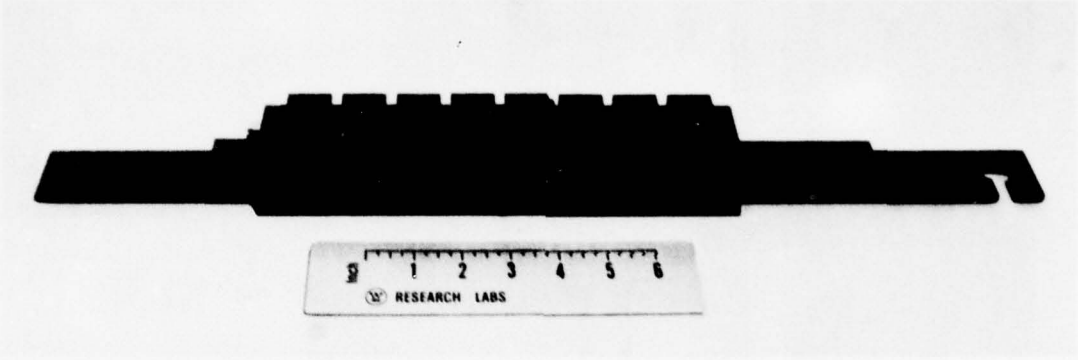

Figure 3.2 Eight-bin graphite sliding boat

During the course of this investigation 32 epitaxial layers were produced to provide data on our doping and thickness control as well as supplying wafers for device processing. The desired multi-layer structure of p-type AlGaAs on n-type GaAs on a semi-insulating GaAs substrate was grown by both LPE-AlGaAs on VPE-GaAs and by LPE-AlGaAs on LPE-GaAs. Due to the difficulty of controlling the thickness of the VPE-GaAs layer after the inevitable melt-back during subsequent LPE growth, the all-LPE technique gave faster results and more-usable wafers.

3.1 Thickness Control

One of the critical problems associated with the epitaxy of the JFET heterostructure is thickness control. This stems from photolithographic requirements (i.e., aspect ratio for gate definition), and the operation of the device in the enhancement mode, i.e., the channel is normally pinched off by the built-in junction potential. LPE growth was accomplished in a multi-bin graphite slider boat as shown in Figure 3.2. It is well known that epitaxial growth in this type of apparatus is diffusion limited.[2] GaAs LPE growth over wide temperature ranges is understood; however, GaAlAs growth is more difficult to model since there are two diffusing species in the Ga-rich melt. Since the growth dynamics of GaAs are well understood, we are in a good position to satisfy the stringent requirements placed on the GaAs channel. Additionally, it turns out that GaAlAs grows at a slower rate than GaAs, hence the GaAs growth parameters are more stringent than those for the GaAlAs.

GaAlAs enters into the thickness consideration mainly due to problems with Al in the liquid melt. Researchers involved in electro-optic

applications of GaAlAs have determined that heavily doped GaAlAs growth is best achieved at temperatures of 800°C or higher. To try and insure good control of the GaAs channel thickness, it is desirable to slow the growth rate of the GaAs as much as possible by having as low a starting temperature as is consistent with the GaAlAs growth criteria. We therefore set 800°C as an upper bound on system temperature. To aid in thickness control, it is advantageous to commence active layer growth from a melt where growth has previously been established. We determined that a 0.3μ active channel could be grown using the following sequence:

(1) n^- GaAs melt exactly saturated at 800°C on a GaAs source crystal.

(2) Using a cooling rate of 13°C/hr, deposition started on the source wafer. After 1°C of cooling, the semi-insulating substrate is slid under the melt and growth continues for one minute. At this point, the substrate is moved to the GaAlAs position.

We have determined that $Ga_{.4}Al_{.6}As$ grows approximately one-half as fast as GaAs for the conditions just described. Because of aspect ratio considerations, it is desirable to limit the gate layer to no more than one micron of thickness. Additionally, as is later described, it is useful to consider a p+ GaAs cap on the GaAlAs gate. Given the growth conditions just reviewed, it is easy to grow 0.5μ GaAlAs and 0.5μ GaAs gate layers as well as the 0.3μ active channel.

3.2 Doping Control

The proposed device required a 6-9 x $10^{16}/cm^3$ n-type GaAs active layer and a p^+ AlGaAs gate junction. Active layer doping is a fairly straightforward process, since Sn is a slow diffusing, well-behaved donor. Figure 3.3 shows the relationship of the Sn dopant in the Ga/GaAs melt to the doping level in the epitaxial layer with the growth temperature as a parameter. For the high doping required by the device, it was quite easy to reproducibly obtain the desired doping level to within 10% accuracy. We then had to establish the appropriate quantities of dopant and Al to produce the desired p layers of GaAlAs. Because the desired properties of the heterostructure rely on a hyper-abrupt hetero interface, it is necessary to carefully review the selection of dopants. Group II elements, which yield p type electrical behavior (i.e., Cd or Zn), are known to be fast diffusers in GaAs. Ge, an amphoteric Group IV element which incorporates predominantly on As sites in LPE growth and is a slow diffuser, was selected as being most suitable for our heterostructure device. However, there is a functional relationship between the p doping level and the AlAs mole fraction in the GaAlAs crystal. Figure 3.4 gives doping as a function of AlAs mole fraction for several dopants after the work of Cheung at Stanford University.[3] The range of growth temperatures employed was 840 - 810°C, so these results were a reasonable guideline for the present task. As can be seen from

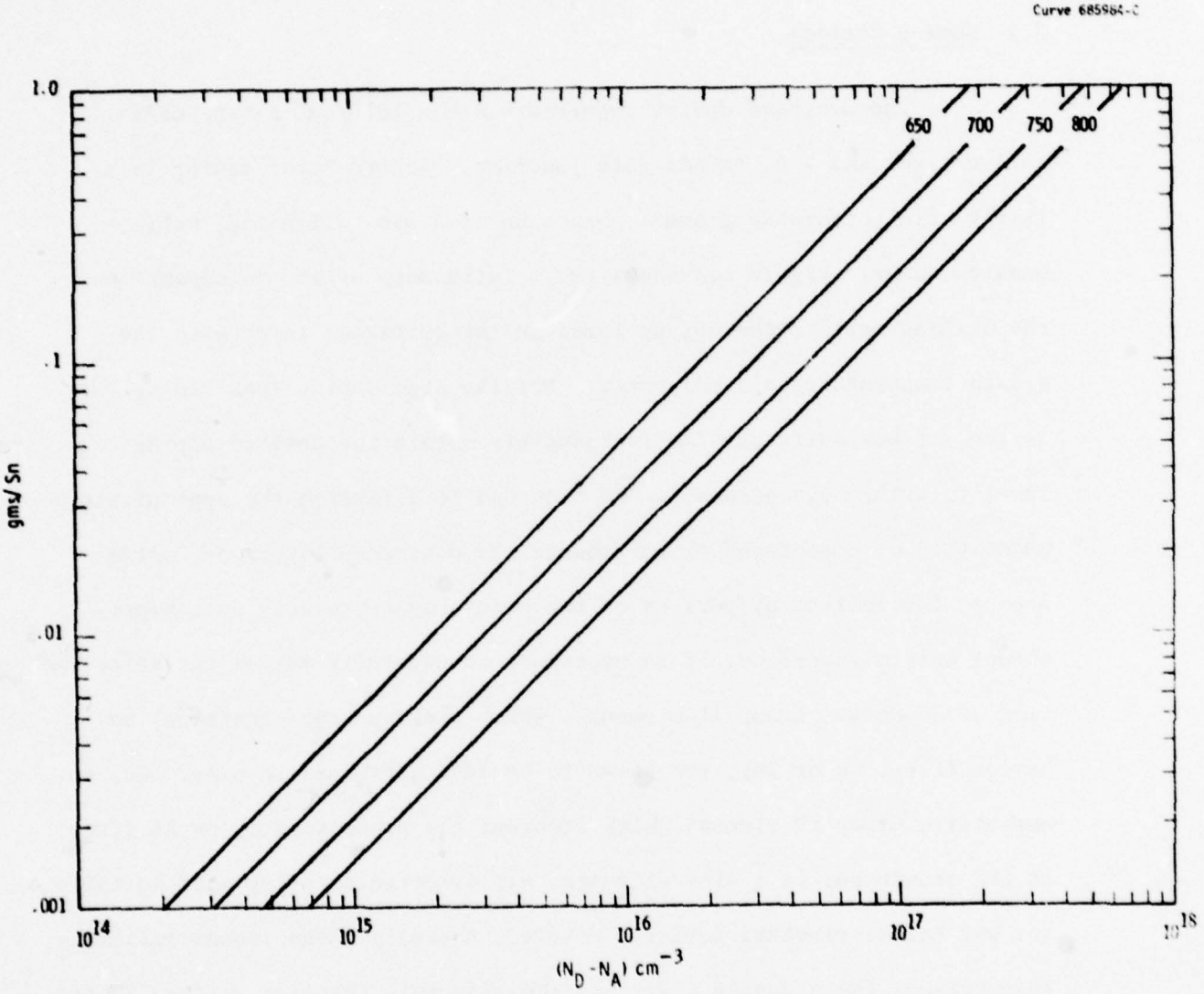

Figure 3.3 Grams of Sn needed to achieve particular doping level in 5 gm Ga melt with growth temperature as a parameter

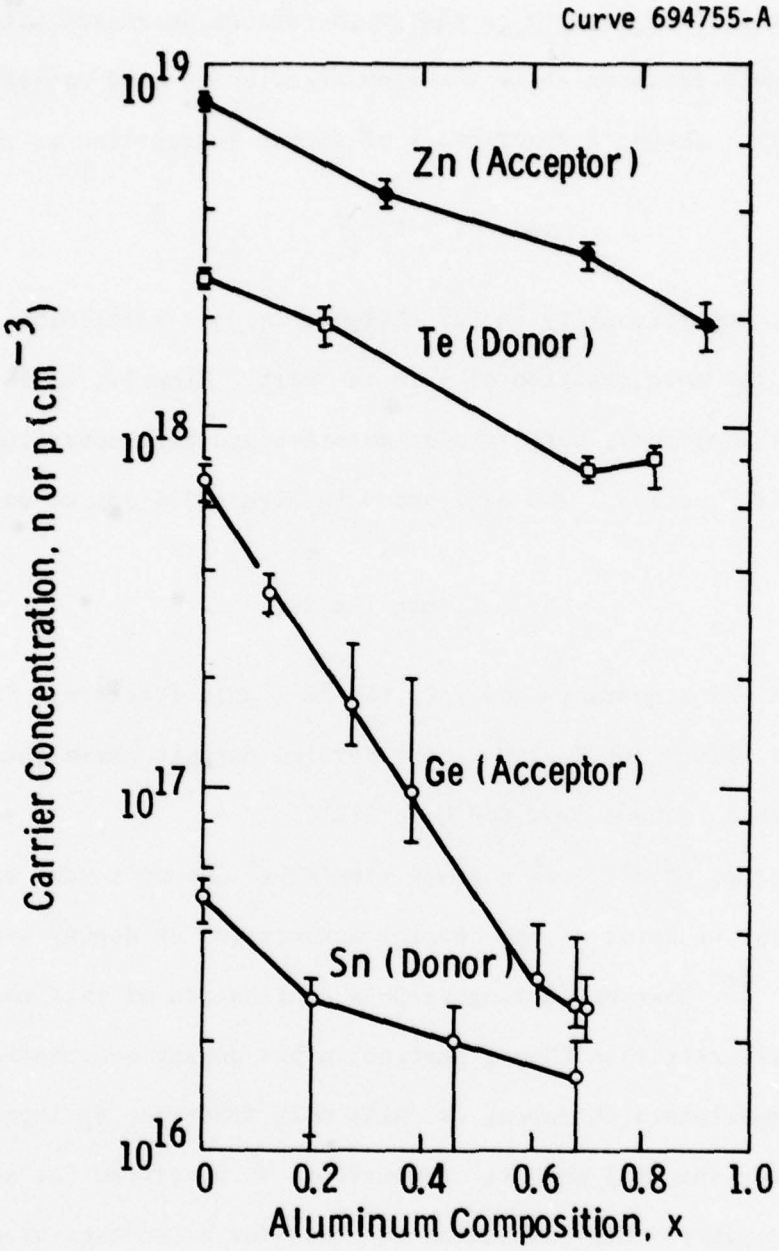

Fig. 3.4— Carrier concentration vs. aluminum arsenide concentration for Ga Al As grown between 840 - 810 °C. The mole % of dopant in the melt is fixed at .5%. (after Cheung)

the graph, the carrier density in the grown crystal decreases with increased AlAs mole fraction while the atom fraction is held constant in the liquid melt. Cheung's description of doping segregation is given as

$$p(\text{or } n) = K_i X_i^{\ell},$$

where K_i is a proportionality factor characterizing a particular impurity i, and X_i^{ℓ} is the mole fraction of i in the melt. Clearly, K_i is affected by growth temperature, substrate orientation and melt constituents, i.e., AlAs mole fraction. The data shown in Figure 3.4 can be described as

$$K_i = \tilde{K}_i \exp(-a_i x),$$

where $\tilde{K}_i$ and a_i are constants and x is the AlAs mole fraction. Table 1 shows Cheung's values for $\tilde{K}_i$ and a_i for several dopants where the temperature of growth ranged from 840°C to 810°C.

Springthorpe, et al., did a study similar to Cheung's work and observed similar behavior of the carrier density for Ge doping vs. AlAs mole fraction.[4] However, Springthorpe's explanation of this phenomena is somewhat different than Cheung implied in his dopant description. Besides the experiments on doping vs. AlAs mole fraction, Springthorpe took resistivity and Hall data vs. temperature to determine the activation level of the dopants. His conclusion was that for a constant atom fraction of Ge in the liquid melt, a constant amount of Ge is incorporated in the grown crystal; hence, segregation is not a function of AlAs mole fraction. Instead, he found that the Ge ionization energy is a function of AlAs mole fraction. This is not a trivial distinction, for it implies a Ge doping limit for high AlAs mole fraction. Based on this work,

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TABLE I

DOPANT CHARACTERISTICS IN $Al_xGa_{1-x}As$ LAYERS AS A FUNCTION OF Al COMPOSITION

Dopant	$K = \tilde{K}_i \exp -(a_i x)$
Zn	$1.6 \times 10^{19} \exp(-1.49x)$
Ge	$1.4 \times 10^{18} \exp(-5.28x)$
Te	$5.0 \times 10^{18} \exp(-1.64x)$
Sn	$9.6 \times 10^{16} \exp(-3.17x)$

we endeavored to determine an upper limit on p-type carrier concentration for 60% AlAs mole fraction in the grown crystal. As previously discussed, all growth experiments were performed at 800°C. Figure 3.5 shows p-type doping as a function of the ratio of Ge to Ga weights for liquid melts constructed to yield 60% AlAs. The effective segregation coefficient, i.e., the relationship between electrically active acceptors at room temperature and the atom fraction of impurities in the melt, is given as K_{eff}, where

$$K_{eff} = \frac{P_{RT}}{\text{Atomic Concentration of Ge in Melt}}$$

From Figure 3.5 one can obtain $K_{eff} = 3.59 \times 10^{-5}$. A similar study was performed on GaAs, with the resulting segregation coefficient equal to 3.49×10^{-3}. Thus, if one relies on Springthorpe's dopant model along with our empirical results, the following conclusions can be drawn:

(1) If one constructs a melt designed to yield a 60% AlAs epitaxial layer and provides 12% Ge atomic fraction in the melt, the net p carrier density in the grown crystal will be 2×10^{17}.

(2) For a 12% Ge atomic fraction in a Ga-GaAs melt, the net p carrier concentration is approximately 2×10^{19}.

(3) The Ge-doped GaAs example sets an upper bound on the density of Ge atoms incorporated in the $Ga_{.4}Al_{.6}As$ example.

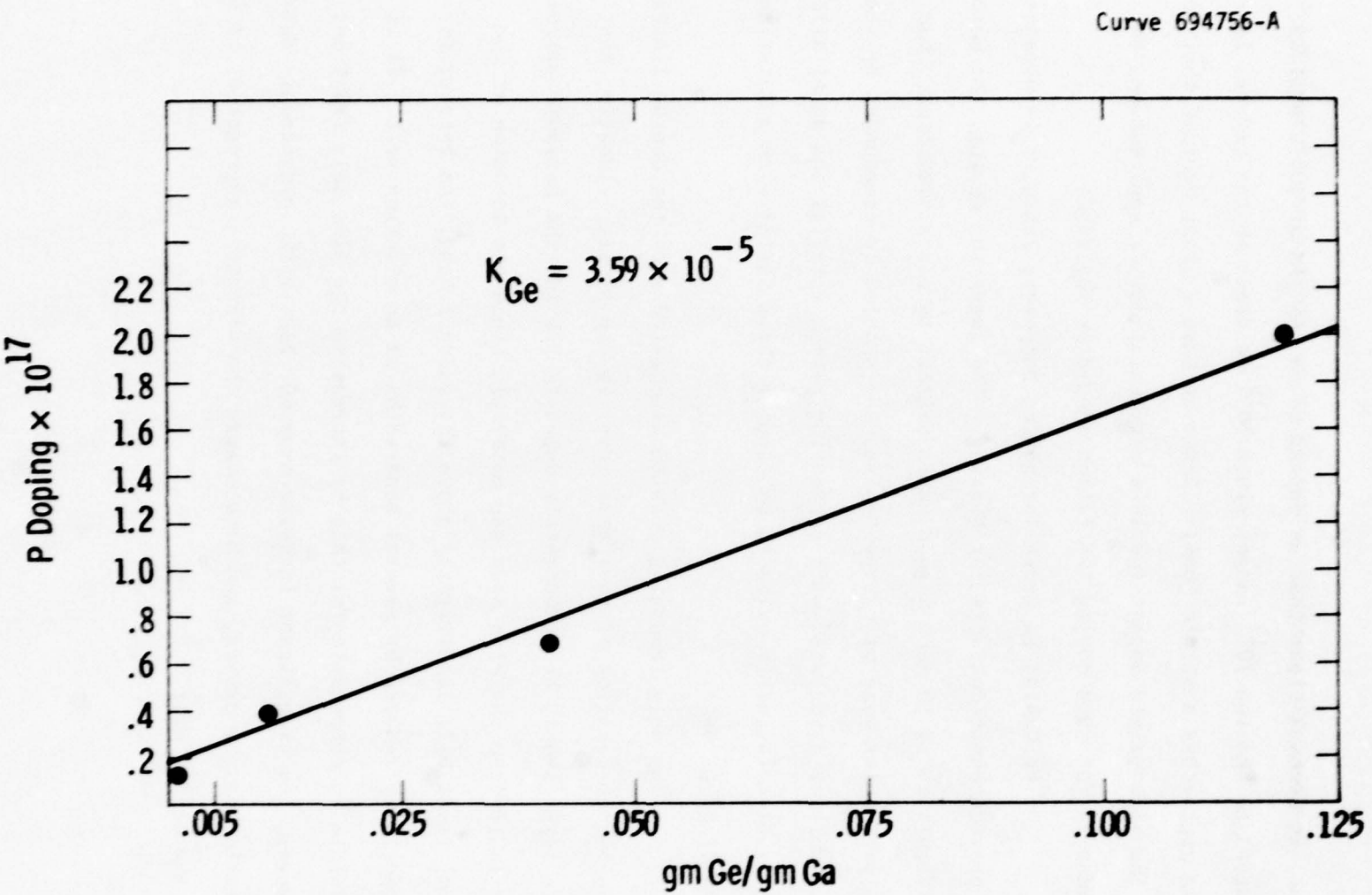

Fig. 3.5 – P-carrier concentration vs. Ge/Ga by weight for 60% AlAs mole fraction with growth at 800°C

Thus, it becomes clear that Ge doping of $Ga_{.4}Al_{.6}As$ at 800°C will be limited to the low 10^{17} range, since 10^{19} Ge atoms in the crystal lattice approaches a strain level. Since we have already decided that Ge is the appropriate dopant for this particular device application, the tradeoffs for this doping limitation should be reviewed.

The GaAlAs is grown for gating purposes; hence, it is necessary to provide ohmic contacts for biasing. The lower the doping, the more difficult it is to make a good ohmic contact to a semiconductor. For the particular case of p-type GaAlAs, the problem is compounded by the difficulties associated with contacting p-type material and an Al alloy. The problem is easily overcome by capping the p GaAlAs with a solution contact of p^+ GaAs.

The only remaining problem associated with the doping limitation is the location of the Fermi level in the p gate. Ideally, the gate layer should be degenerately doped to provide the maximum barrier available from the wide band gap material. Since the location of the Fermi level will lie slightly above the valence band, the barrier is effectively reduced by several hundredths of an electron volt. It is possible to compensate for this by increasing the AlAs mole fraction; however, any significant increase over 60% AlAs risks hydroscopic deterioration of the device, and also lowers the effective segregation of Ge in the GaAlAs melt.

4. DEVICE FABRICATION

Two fabrication processes were used to produce heterojunction transistors during this program. The first devices, called Mark I, used a three mask scheme while later devices, Mark II, required four masks. The extra mask step provided an extra oxide layer which reduced the parasitic input capacitance of the Mark I. Both fabrication sequences used ion-beam milling as well as selective etching of AlGaAs on GaAs to form an AlGaAs gate finger separating two AuGe contacts on the GaAs layer.

4.1 Mark I Device

The three mask fabrication sequence for the Mark I device is shown in Figure 4.1. The starting material is a semi-insulating GaAs wafer on which two epitaxial layers have been grown. The first layer is n-type GaAs with a doping of 8×10^{16} cm^{-3} about 1700Å thick. This is covered by a 5000Å thick epi-layer of p-type AlGaAs. After evaporating a contact metal on the AlGaAs, the first mask is used to isolate the active device regions by ion-milling down to the semi-insulating substrate in Fig. 4.1(B). The second mask defines the gate stripe in the gate metal. The p-type AlGaAs is then ion milled nearly into the n-type GaAs layer using the gate metal as a mask. A chemical etch is used to preferentially etch the AlGaAs and stop at the GaAs layer as shown in Figure 4.1(C). The ion-milling of the n-GaAs must be avoided since the ohmic contacts deposited on an ion milled surface are inferior to those produced on an etched

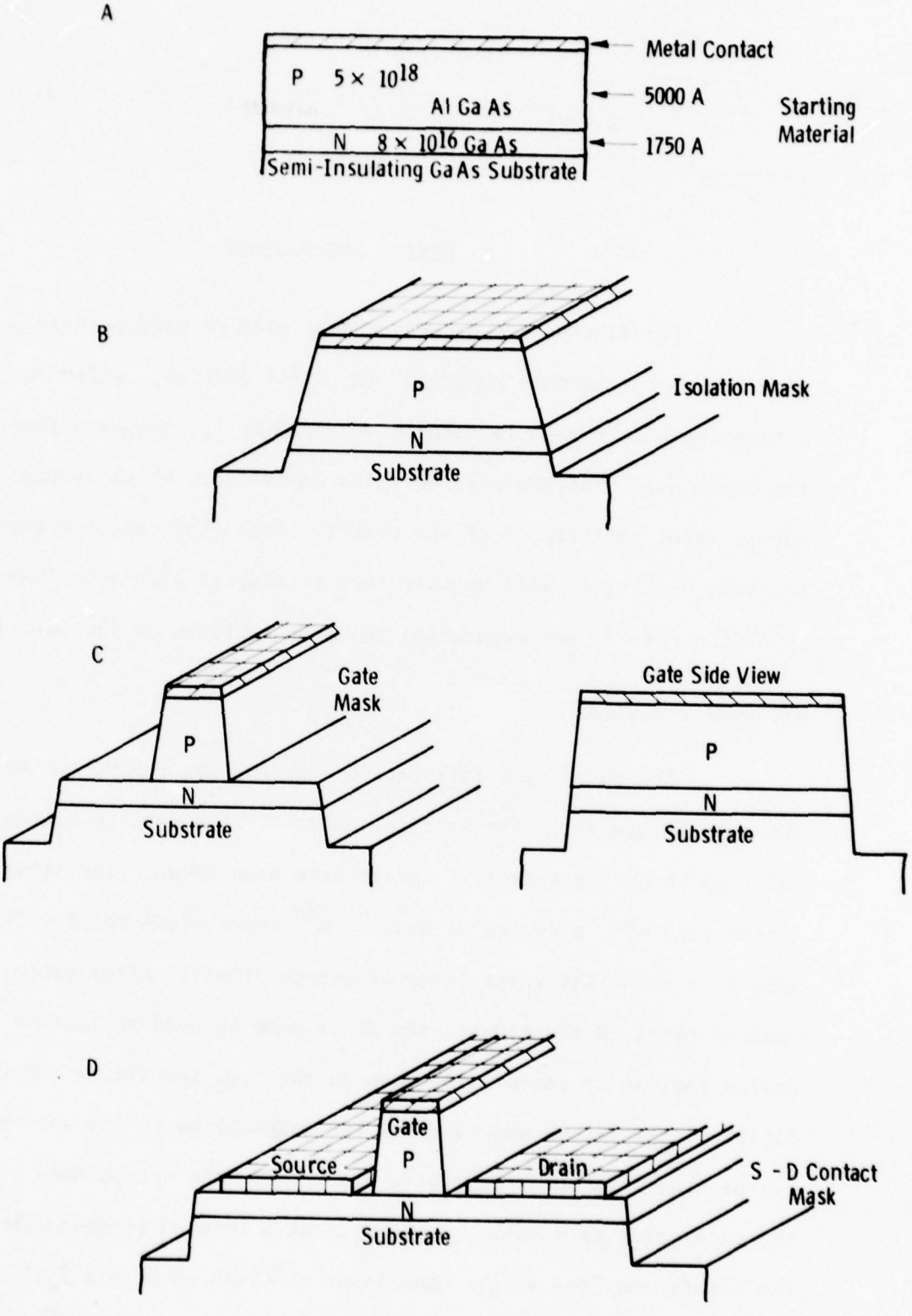

Fig. 4.1 – Fabrication sequence for the Mark I JFET

surface due to surface damage caused by the ion beam. The use of ion beam milling for most of the AlGaAs removal assures good edge definition for the gate. The last mask step, shown in Figure 4.1(D), uses a photoresist rejection to form the Au-Ge source and drain contacts. These are alloyed in a stream of argon and 10% hydrogen using a controlled temperature cycle with a peak of 450°C. Figure 4.2 shows the mask set used for the Mark I device.

4.2 Mark II Device

The Mark I device suffers from a large parasitic capacitance contribution to the input and feedback capacitances. This is illustrated by the sketch Figure 4.3(A). The gate pad lies on the p-type AlGaAs epi-layer and its large area produces a substantial capacitance. This capacitance appears as a parasitic contribution to Cgs and Cg_D as sketched in the figure due to the conductivity of the GaAs epi-layer underneath.

The solution to the excess capacitance is to bring the gate pad off the n-type GaAs mesa and down onto the semi-insulating substrate. This process can be accomplished by using one additional mask step to provide a SiO_2 layer lying over the substrate and going up onto the gate region of the transistor as shown in Figure 4.3(B). The metal on these gate pads is delineated by the source-drain contact mask step as shown in the process sequence for the Mark II devices, Figure 4.4. The oxide mask and the source-drain contact mask are shown in Figure 4.5. Note that the source-drain mask has circular dots in the gate regions to form the gate

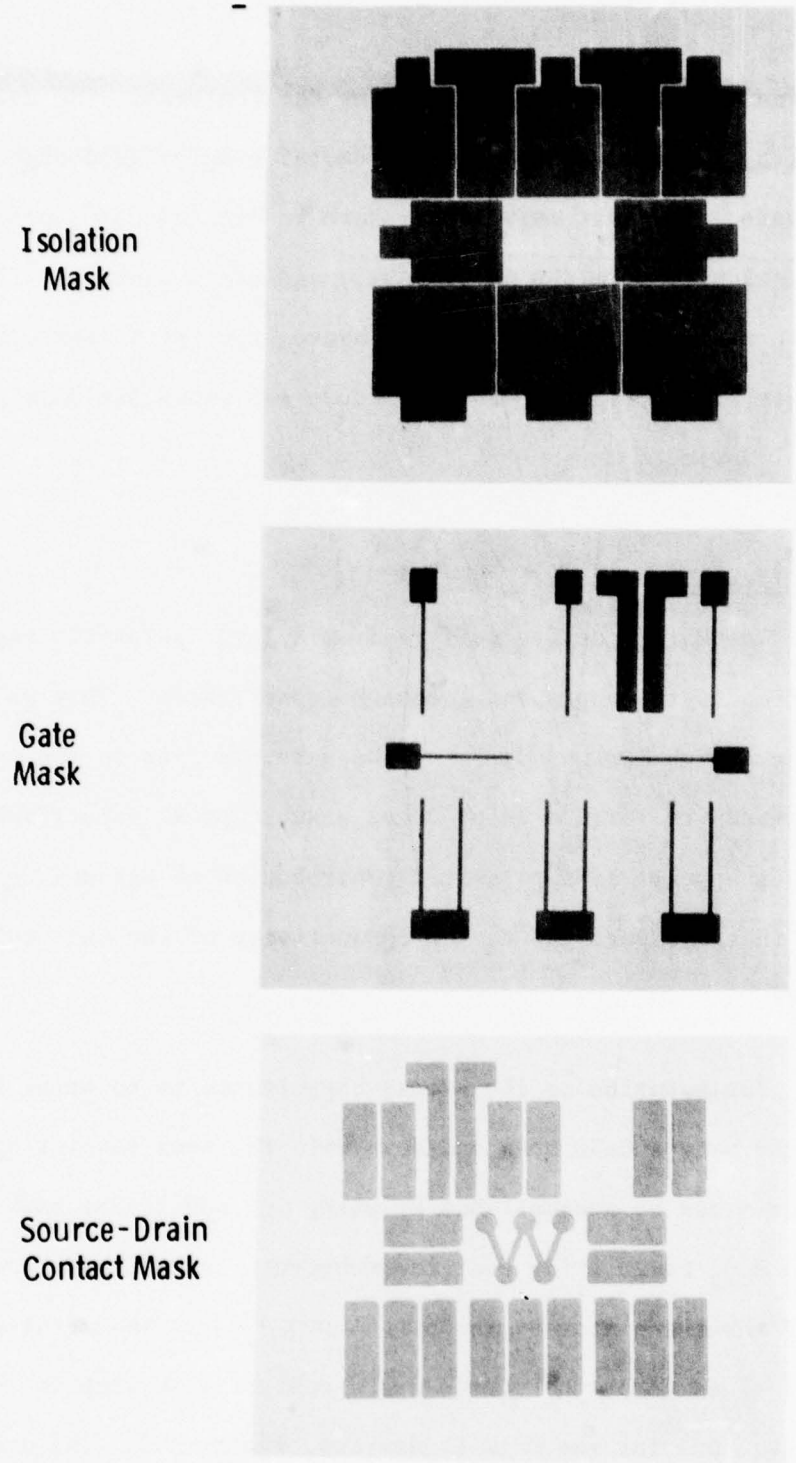

Fig. 4.2—Mask set for Mark I heterojunction FETs

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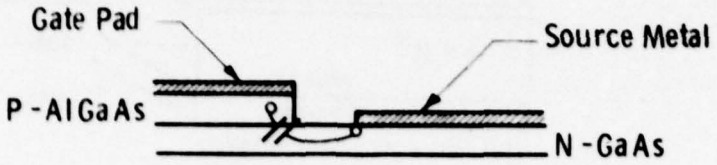


Cross-Section Detail of Parasitic Gate-Source Capacitance

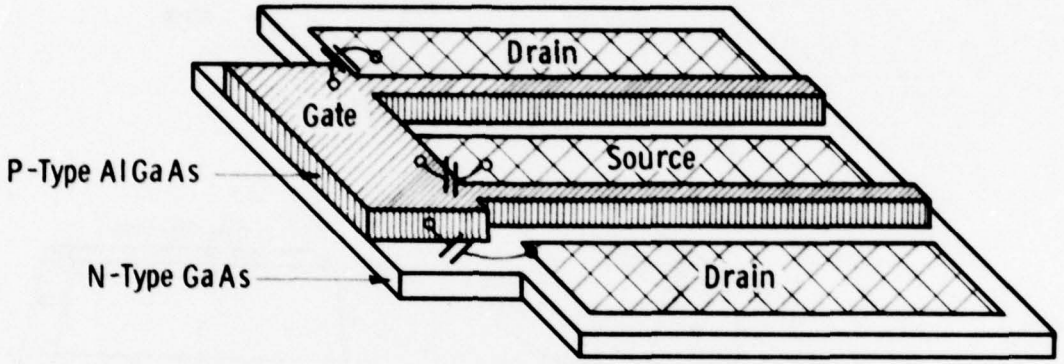


Fig. 4.3a

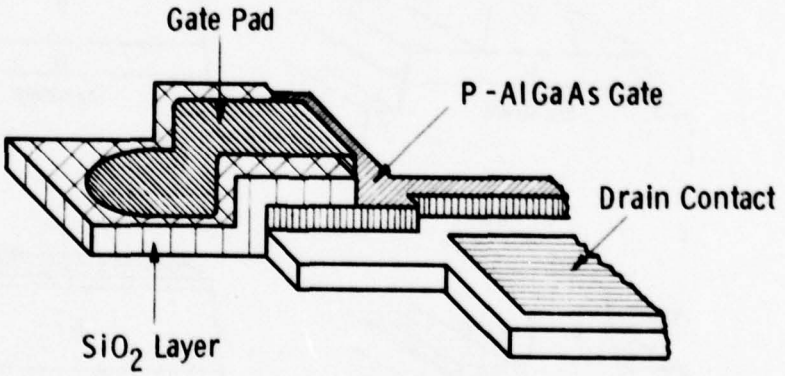


Fig. 4.3 – Structural differences between Mark I and Mark II JFET's

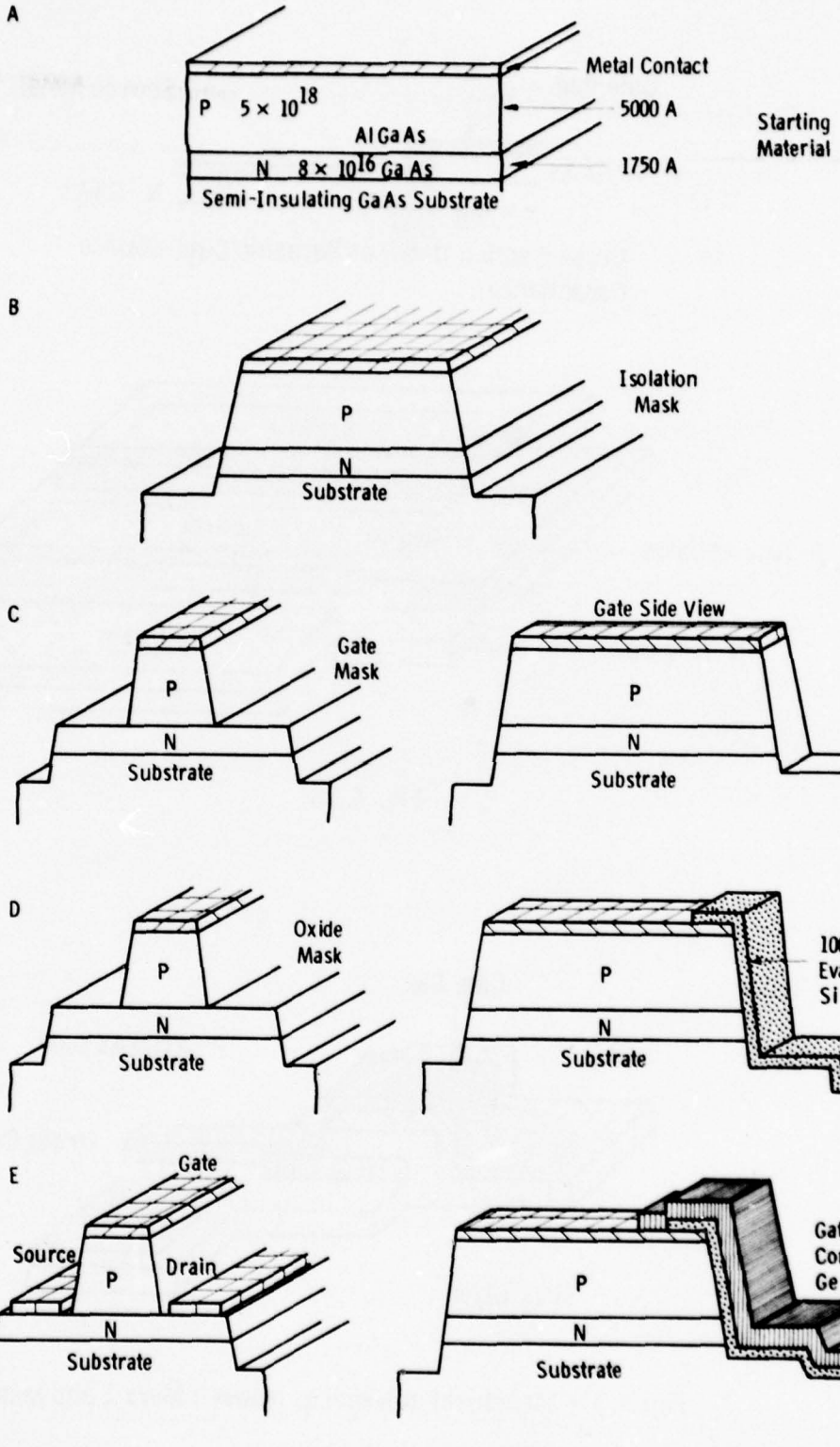
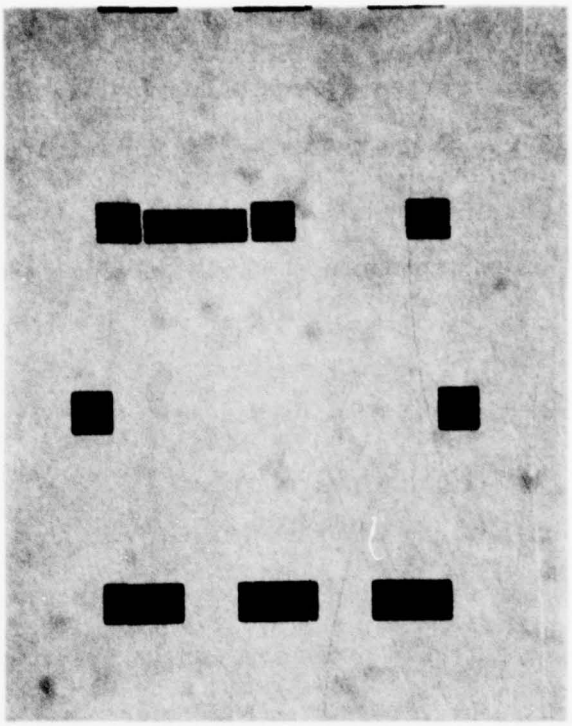
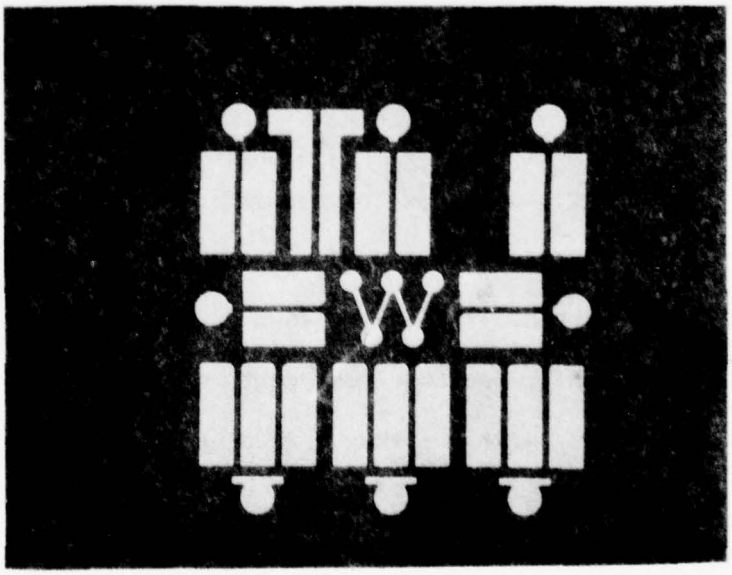


Fig. 4.4 – Process sequence for Mark II JFET's



a) Oxide Mask



b) S - D Contact Mask

Fig. 4.5—Oxide mask and source-drain contact mask for Mark II heterojunction FETs

pads. These pads are shown in completed devices in Figure 4.6. The dark area is the SiO_2 pad while the circular or semi-circular metal is the gate pad formed by the source-drain lift-off. It extends to the right, down off the SiO_2 and contacts the gate metal on the p-AlGaAs layer underneath.

Two photographs of finished Mark II devices are shown in Figure 4.7. Each module consists of eight FETs of 300 μm, 150 μm and 120 μm periphery. These devices had gate lengths of 3 μm and 7-9 μm source-drain spacings. The gate definition is good although the sloping sides of the ion-milled p-AlGaAs region produce a longer gate than originally desired. The gate and drain characteristics of devices from two different runs can be seen in Figures 4.8 and 4.9. The gate of device #4-7 in Figure 4.8 shows 2μA of forward current at 2μ. The drain current is not pinched-off at V_{GS}= 0 due to a thicker n-GaAs layer than desired. Pinch-off of the channel is at V_{GS}= -1.2V. The enhancement action with positive V_{GS} is clearly evident and shows good Ids modulation up to V_{GS} = .8V. With a thinner channel layer this device could operate successfully as an enhancement mode logic switch. The device #6-3 in Figure 4.9 shows a gate current of only 1μA at 3V due to a poor contact to the p-AlGaAs. The output characteristics, however, show a reduced drain saturation voltage and enhancement mode operation up to +.5 gate voltage. The transconductance of both devices was between 2 and 3 mmhos.

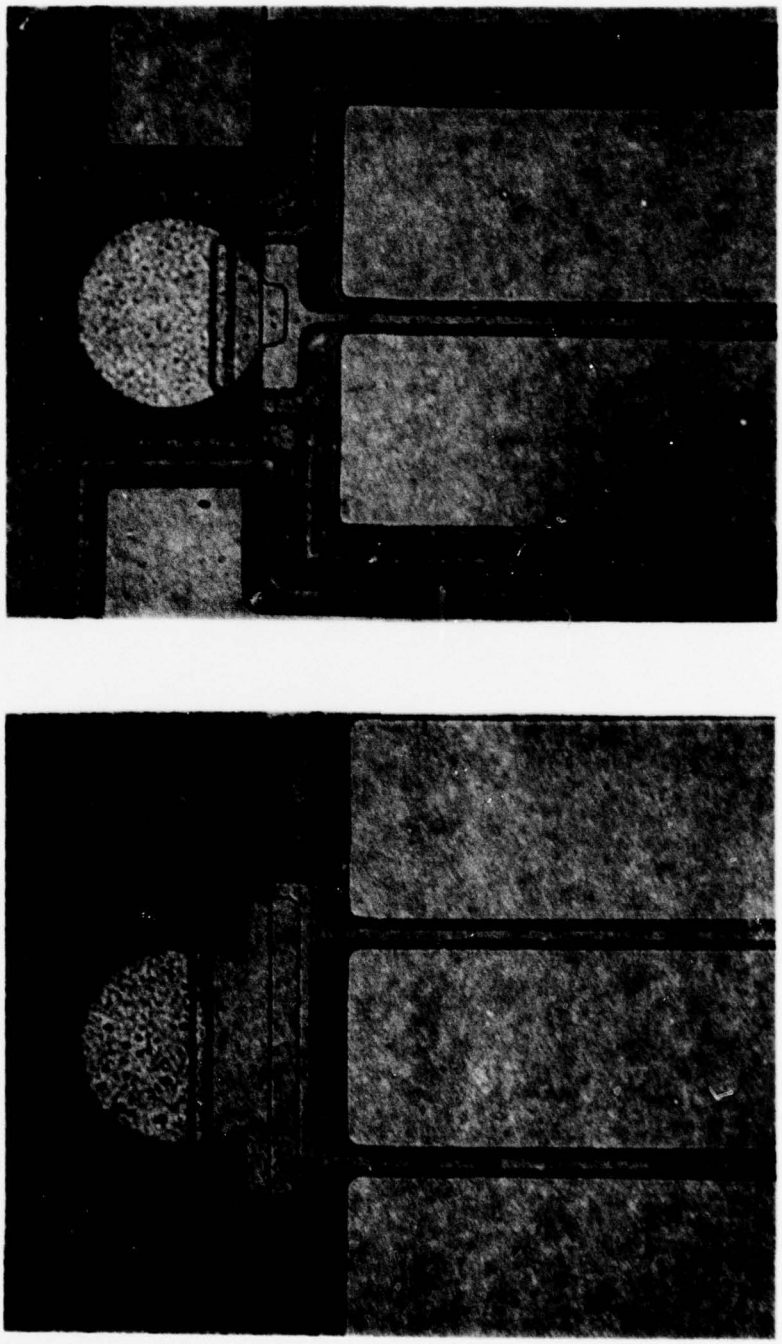


Fig. 4.6—Examples of SiO_2 isolated gate pads on two Mark II heterojunction gate FETs

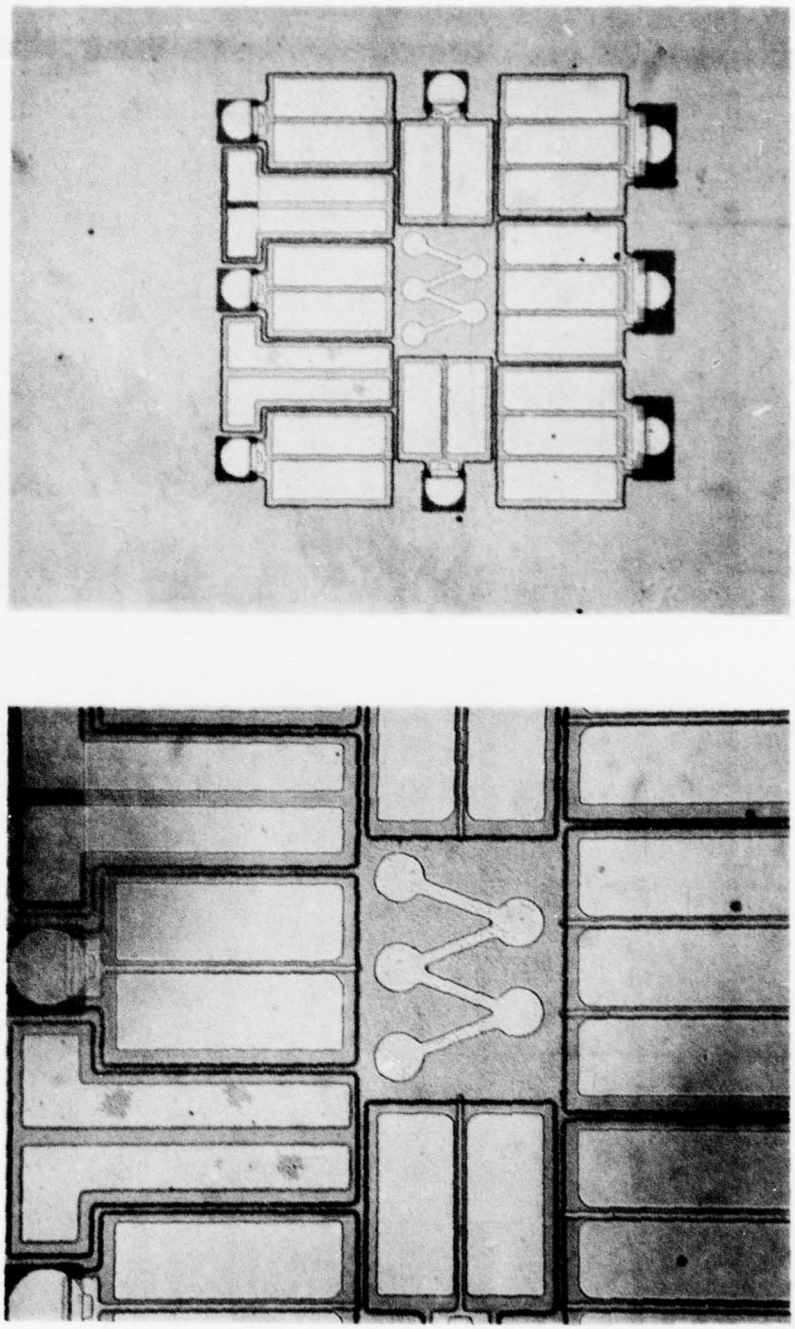
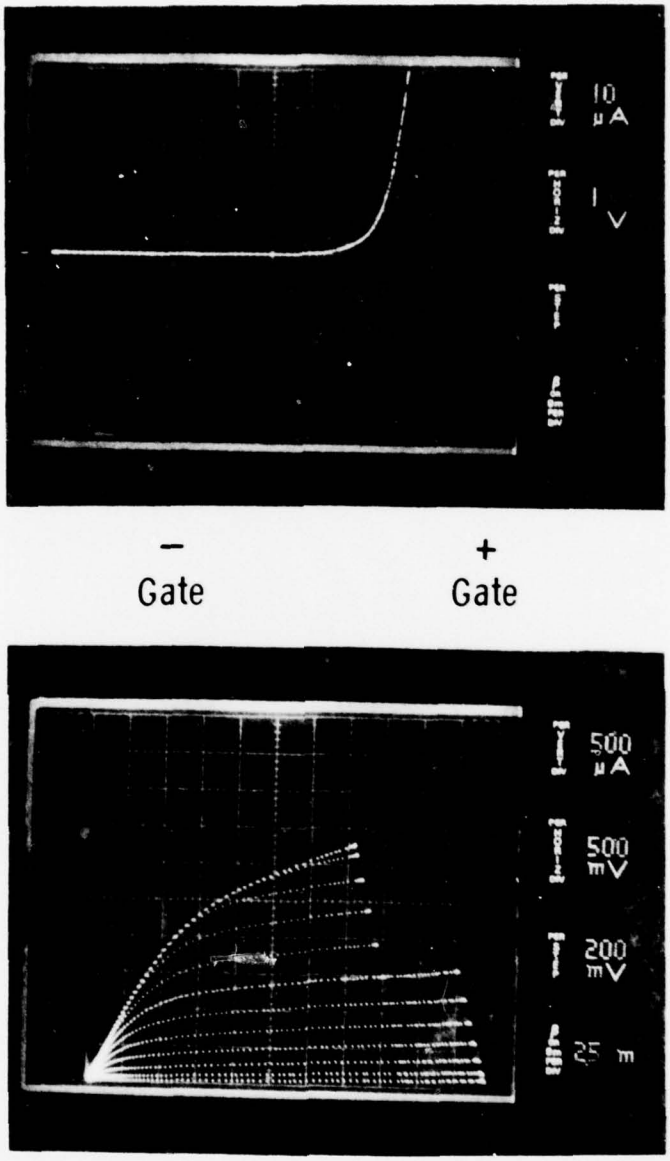
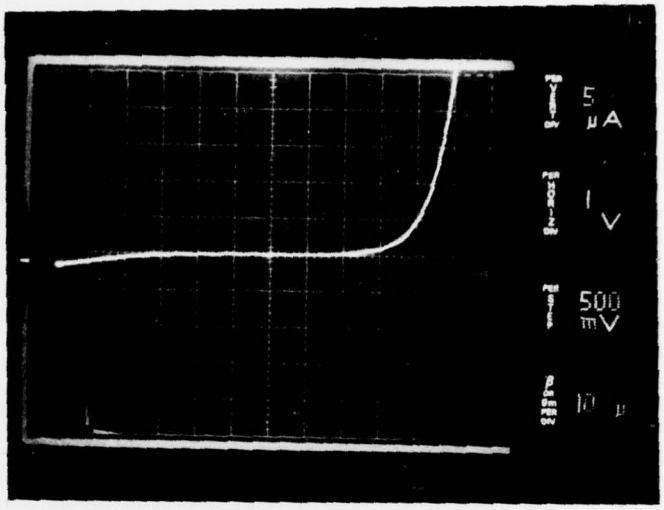


Fig. 4.7—Finished Mark II heterojunction gate FETs



− Gate + Gate

Fig. 4.8—Gate and drain characteristics of Mark II heterojunction FET from run #4. (line with I_{DS} = 1500 uA at V_{DS} = 4 v is V_{GS} = 0)



−
Gate

+
Gate

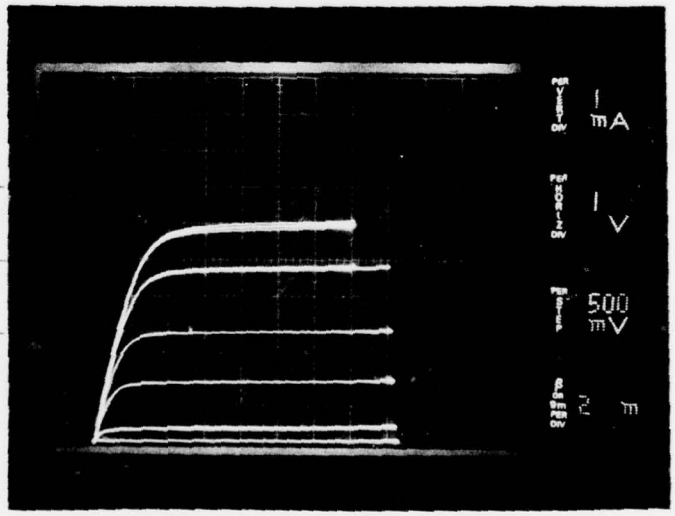


Fig. 4.9—Gate and drain characteristics of Mark II heterojunction FET from run #6. (V_{GS} =0 along curve through I_{DS} =4.8 mA, V_{DS} =5V)

5. DEVICE EVALUATION

Devices from each wafer were evaluated using I-V, C-V and s-parameter measurements. The low frequency measurements showed a rectifying contact to the p-type AlGaAs of the gate. This caused the apparent 2 and 3 volt forward drops of the gate junctions. The microwave measurement showed 3 dB gain at 1 GHz.

5.1 Low Frequency Measurements

The I-V characteristics of two devices were shown in Section 4, Figures 4.8 and 4.9. The forward voltage drop in these devices was 2 volts in 4.8 and 3 volts in 4.9, while the maximum usable gate voltage for enhancement operation was below 1 volt. If the 2 volt forward drop was the true forward potential of the p-AlGaAs to n-GaAs heterojunction, then,

a) The enhancement operation of the FET should have continued for forward gate voltages up to nearly 2 volts, and

b) There should not be a device with a 3 volt forward voltage.

Using the voltage dependence of the gate-drain capacitance, the problem was ascertained to be a poor contact to the p-type AlGaAs which added a leaky Schottky barrier junction in series with the heterojunction gate.

A typical C-V curve for these heterojunction gate devices is shown in Figure 5.1. For negative gate voltages, the heterojunction is reverse biased and the capacitance drops rapidly until the FET is pinched-off at V_{GS}=-.75 to -1.0 volts. For positive gate voltages, the capacitance decreases (instead of increasing) out to about 2.5 volts after which it rises rapidly. This behavior is caused by a depletion region under the metal contact to the p-AlGaAs. As positive gate voltage is applied, the reverse biased contact absorbs the increasing voltage and its increasing depletion width into the p-AlGaAs causes the capacitance to decrease. Above 2.5 volts, the poor contact breaks down and the rapidly increasing capacitance of the forward-biased heterojunction is again apparent.

The gate I-V characteristic with the poor ohmic contact to the p-AlGaAs can be summarized as shown in Figure 5.2. Figure 5.2(a) shows the expected heterojunction behavior with a forward voltage drop of -1.5 volts and low reverse current. The poor Schottky contact on the p-type AlGaAs gives a good forward characteristic for negative voltages and a leaky breakdown for positive voltages of 1.0 to 2.0 volts as shown in Figure 5.2(b). The composite I-V characteristic of both junctions in series [Fig. 5.2(c)] has low leakage for negative gate to source voltages and a high forward drop due to forward biasing the heterojunction and breaking down the poor Schottky contact.

5.2 RF Performance

Since the devices fabricated were not completely pinched-off or self-depleted with no gate bias, no attempt was made to bond adjacent

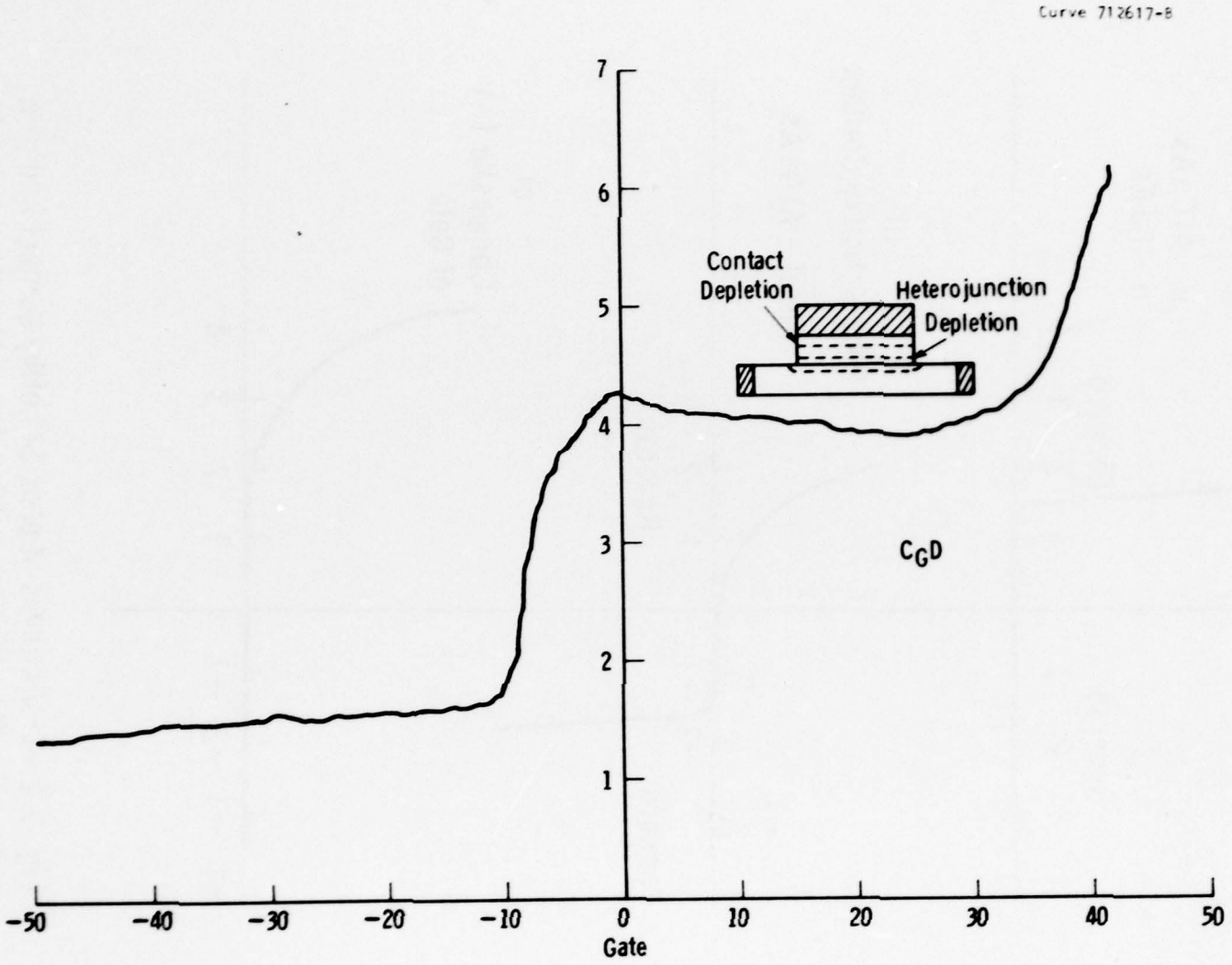


Fig. 5.1 – Gate to drain capacitance of heterojunction gate FET as a function of gate-drain voltage

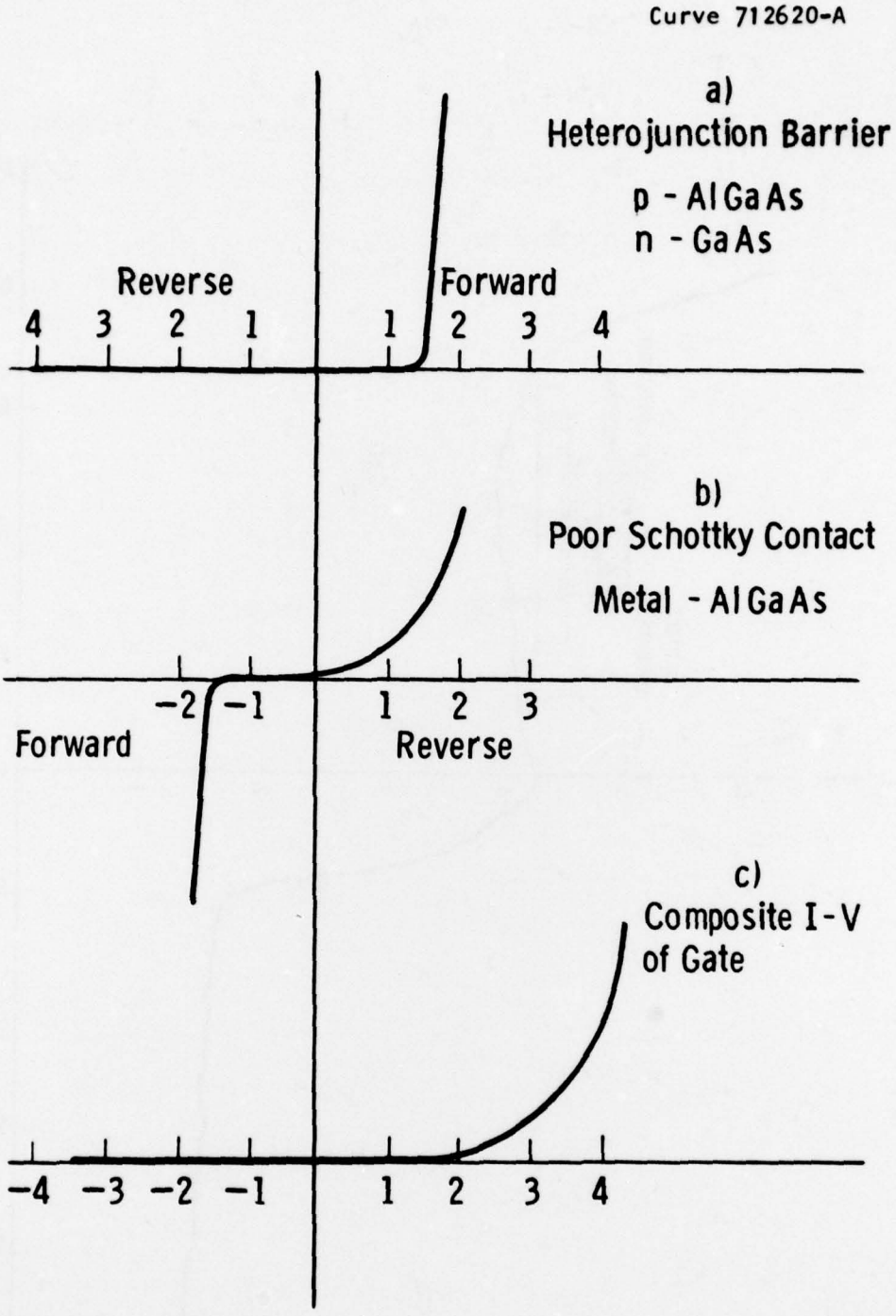


Fig. 5.2—I-V curves of poor Schottky contact and p-n heterojunction leading to high forward voltage behavior

devices into a switching circuit configuration to test delay times and rise times. Individual devices were bonded into microstrip-based headers and tested by measuring their small signal s-parameters. The s-parameters of a typical device as listed in Table 5.1.

Measured S-Parameters and Gain

Heterojunction FET #6-2G

Lg = 3μm, WG = 300 μm

Frequency, GHz	S11	S12	S21	S22	MSG	MAG
0.5	0.94/-43°	0.0008/40°	0.275/110°	0.97/-41°	15.3dB	9.7dB
1.0	0.91/-94°	0.013/-18°	0.196/50°	0.94/-99°	11.8dB	3dB

The calculated maximum available gain for this device is 3dB at 1GHz and 9.7dB at 500 MHz with a cutoff frequency, f_{max}, of 1.5GHz. The maximum stable gain, MSG, is 11.8dB at 1GHz and 15.3 dB at 500 MHz. These are reasonable performance values for a device with gate lengths of 3-4 μm.

6. CONCLUSIONS AND RECOMMENDATIONS

The work that has been carried out on Contract N00014-76-C-0735 produced a heterojunction gate FET using a p-type AlGaAs gate on n-type GaAs. These devices showed power gains of 3 dB at 1 GHz and 9 dB at 500 MHz. A number of areas were successfully pursued, including:

A. An LPE growth system was used to grow the n-GaAs/p-AlGaAs structure required for the devices. Good control of the doping densities and surface morphology was achieved with submicron GaAs layers and micron thick AlGaAs layers. The use of Ge to dope the AlGaAs resulted in acceptor concentrations of 2×10^{17} cm^{-3}.

B. The selective etching of AlGaAs and the ion milling of AlGaAs were both employed in the device fabrication. The ion milling allowed accurate formation of the gate geometry and proved controllable and reproducible. A selective etch for AlGaAs in the presence of GaAs was needed to finish the gate formation since ion milling the GaAs surface before applying ohmic contacts resulted in high contact resistance.

Some areas of device fabrication were identified as a problem. The ohmic contact to p-type AlGaAs was never completely ohmic and resulted in forward voltage drops for the heterojunction diode in excess of those predicted by band theory considerations. Referring to the heterojunction band structure of Figure 6.1, the built-in voltage can be calculated by

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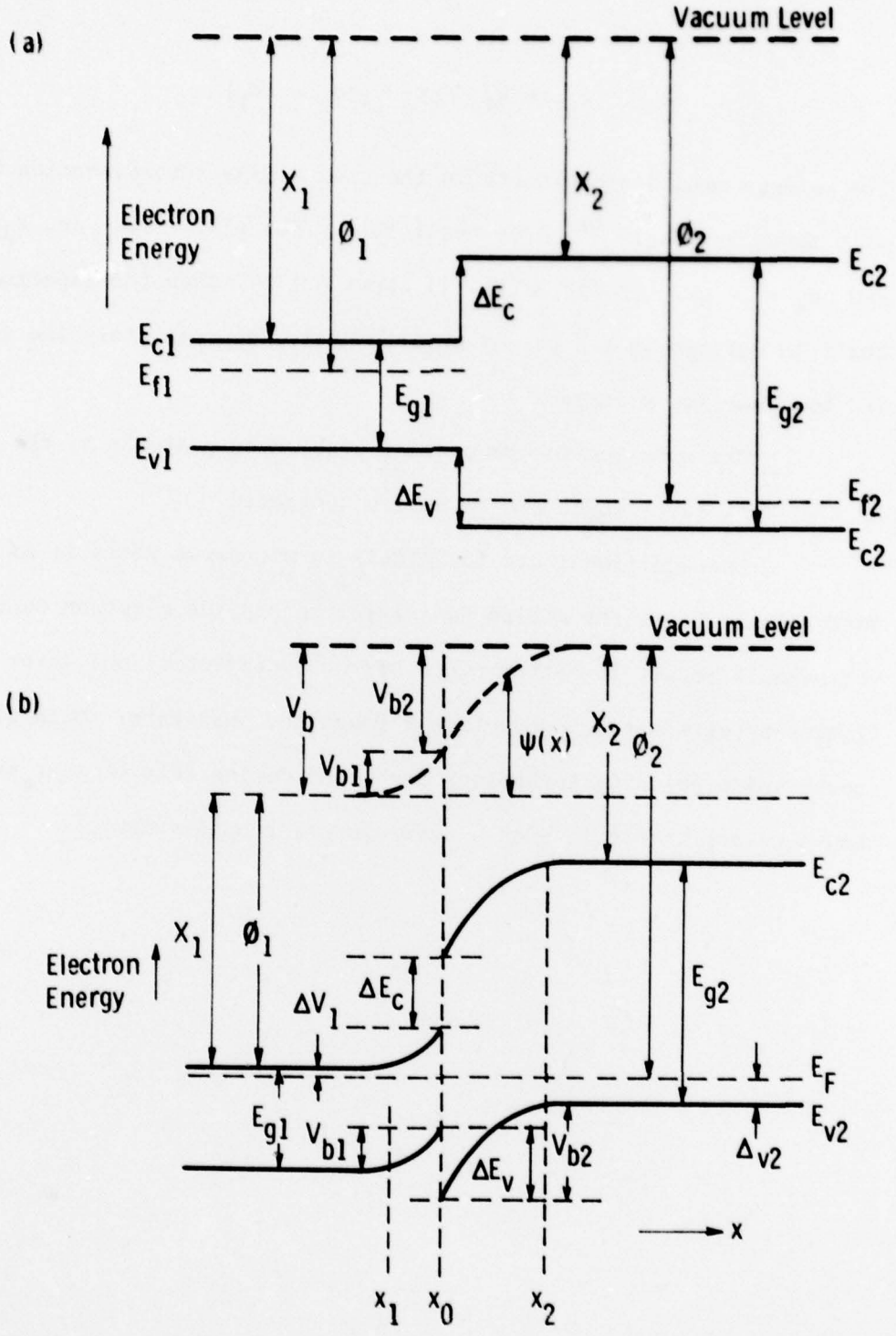

Fig. 6.1—Energy ban diagrams for two isolated semiconductors (a) and (b) for n-p hetero-junction at equilibrium (no external voltage applied) (after Anderson [5])

$$V_{Bi} = E_{g_2} - \Delta E_c - (\Delta V_2 + \Delta V_1) .$$

The valence band discontinuity in the GaAs-AlGaAs heterojunction has been shown by Dingle[6] to be negligible. For $p^+ - Al_{.3}Ga_{.7}As$, $E_{g_2} = 1.8$ eV and $E_c = .4$ eV. If $(\Delta V_1 + \Delta V_2)$ is about 0.1 eV, then the expected built-in voltage is 1.3 eV, or unfortunately, approximately the same as the homojunction voltage.

The solution to the contact problem on p-AlGaAs is the growth of a p^+-GaAs layer which can be easily contacted.

One additional use for AlGaAs in microwave FET's is as a buffer layer below the active GaAs layer to provide electron confinement. This should result in better pinch-off characteristics and lower noise figures by eliminating conduction through the substrate. Much of the growth and processing technology developed during this current program should be applicable to such a heterojunction buffer device.

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